Listing of Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

1. (Previously Presented) A method for manufacturing ROM memory devices, the method comprising:

forming a trench isolation structure within a cell region of a semiconductor substrate, the cell region being in an array region for ROM memory devices, the trench isolation structure being provided to separate a continuous bit line region of the cell from another continuous bit line region from another cell;

forming a gate structure within the cell region;

forming a first sidewall spacer overlying a first side of the gate structure and a second sidewall spacer overlying a second side of the gate structure, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being configured to-extend over and overlap a portion of the trench isolation structure and to extend over and overlap a portion of source/drain regions, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being adapted to separate the gate structure from the trench isolation region and to separate the gate structure from the source/drain regions;

applying a refractory metal layer overlying the gate structure including the first side wall spacer and the second sidewall spacer and exposed portion of the trench isolation structure;

alloying the refractory metal layer to the gate structure and exposed portions of source/drain regions to form silicided regions overlying the gate structure and source/drain regions; and

selectively removing the refractory metal layer from the sidewall spacers and exposed portion of the trench isolation structure.

2. (Original) The method of claim 1 wherein the refractory metal layer is titanium or cobalt.

3. (Original) The method of claim 1 wherein the trench isolation region is an STI region.

4. (Original) The method of claim 3 wherein the STI region comprises silicon dioxide.

5. (Previously Presented) The method of claim 1 wherein the memory cell has a channel region using a length of about 0.25 micron and less.

6. (Previously Presented) The method of claim 1 wherein the first sidewall spacer and the second sidewall spacer comprise of a dielectric material.

7. (Previously Presented) The method of claim 1 wherein the buried bit line structure is within the source/drain regions.

8. (Original) The method of claim 1 wherein the trench isolation is within the semiconductor substrate at a predetermined depth, the predetermined depth being greater than a junction depth of the buried bit line.

9. (Original) The method of claim 1 wherein the gate structure has a width of 0.25 micron and less.

10. (Original) The method of claim 1 wherein the array has at least eight cells by eight cells.

11-26. (Canceled)